SEE Test Results for the Snapdragon 820

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***Abstract*— SEE test results are presented for proton, neutron, and heavy ion testing of the Qualcomm Snapdragon 820 and its support DDR4 device (in this case the SK Hynix 24 Gb LP DDR4 device H9HKNNNDGUMUBR-NMH). Processor crashes and DDR4 stuck bits are the primary SEE types for protons and neutrons. Test preparation difficulties and software limitations caused test efforts to be limited to processor crashes, SEFIs and SBU, and Stuck Bits in the DDR4 device. Interpretation of results is complicated by mixing of errors between devices.**

I. Introduction

Smartphones provide the best power to performance ratio of any commercial devices and are of high interest to space users with high risk tolerance, short missions, or low budget. The NASA Electronic Parts and Packaging (NEPP) program has previously studied iPads and other processors for these types of missions, while the NASA PhoneSat program has launched smartphones on CubeSats [1-3].

Figure 1: The Intrynsic Open-Q Snapdragon 820 SOM is shown. Note that the processor is under the SK Hynix LP DDR4 device in the middle. A heatsink is normally placed over the DDR4 device but was unnecessary provided good ventilation was available.

The Qualcomm Snapdragon 820 was tested in a system-on-module (SOM) configuration using the Intrinsyc Open-Q Snapdragon 820 development kit [4]. The SOM includes a Snapdragon 820 SOC with an SK Hynix 24 Gb LP DDR4 (part number H9HKNNNDGUMUBR-NMH [5]) device mounted in a package on package (POP) configuration that did not allow us to directly observe the SOC, and could not be removed for testing, requiring test beams to penetrate both the DDR4 and the SOC. We tested the Snapdragon and attached DRR4 device for heavy ions at Texas A&M University (TAMU), protons at Massachusetts General Hospital (MGH), and neutrons at the Los Alamos Neutron Science Center (LANSCE). Testing was performed allowing the development kit to power the device as designed, because the power system provides many different power rails with a power up sequence that was not available to the test engineers and many of the power connections are made in mid layers of the board. Tools for high-level code development are available but do not have control of the behavior of device resources in a well-controlled way. Our goal for this testing was to have well-controlled operation, so we inserted test software directly into the android boot file, redirecting boot operations directly into our test software at two different points in the boot sequence.

This workshop is organized as follows. Background on the test methods is presented in section II. Detailed test setup is presented in section III. We then present the heavy ion test results for both the Snapdragon 820 and the DDR4 in Section IV. Similar results for the proton and neutron testing are presented in sections V and VI, respectively. Finally, the conclusions are presented in Section VIII.

II. Background

The Qualcomm Snapdragon 820 is an example of a complex system that integrates many components of a modern computer onto a single chip. This type of device, which includes many (but not all) of the integrated circuits required for a computer, is sometimes referred to as a system-on-a-chip (SOC). As an SOC and a complex processor, this device is of considerable interest for the NASA Electronic Parts and Packaging (NEPP) program, and may be a processor of interest for aggressive risk posture missions (such as CubeSats). It also provides a large ant of computing performance at under 10 W. This processor is also of interest because it is made on the Samsung 14 nm LPP (low power plus) fabrication line, which is under consideration for future radiation hardening work.

The Qualcomm Snapdragon 820 is a mobile processor that features four Kryo CPU (central processing unit) cores. It includes the Qualcomm Hexagon 680 DSP (digital signal processor). It also contains the Qualcomm Adreno 530 GPU (graphics processing unit). It is a many-core heterogeneous SOC. A general diagram of the Snapdragon 820 is shown in Fig. 2.

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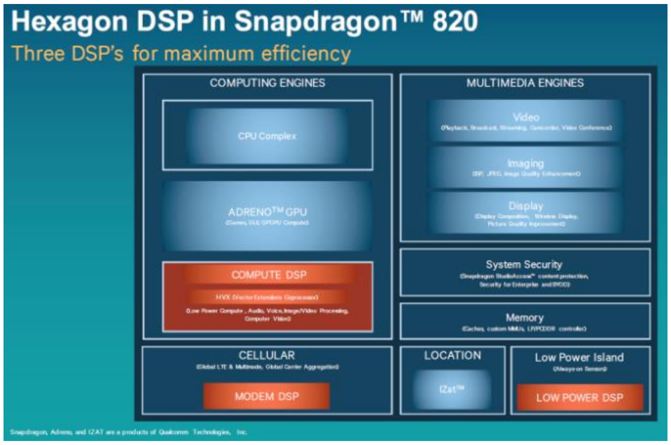

Figure 2: Features in the Snapdragon 820 [1].

Heavy ion and proton testing was performed by exposing a development board to a beam that could penetrate to the active region of the die of the processor (which required also traversing the POP DDR4). We utilized the built-in Android boot code, and some custom code (grafted onto the boot code due to lack of a viable way to write OS-level code). This approach was used to try to capture data on the Android operating system, register upsets, and memory upsets.

It should be noted that the DDR4 device cannot be removed without significant resources to operate the device outside of the normal boot configuration. For this reason, we did not try to remove the DDR4 device. Further, we were able to determine that the entire DDR4 device was thinner than 400 µm, and likely included only a single layer of thin die (DDR-based memory devices typically have 250 µm or thinner die). Because of this we used only beams with long range, with the understanding that the higher LET beams will have significantly reduced reliability in the LET identified based on presumed die thickness.

A key aspect of identifying device sensitivity is normalizing the observations to the test system used. If a simple test system could be used that gave clear ability to read and write registers, then watch them be modified by radiation, then the results interpretation would be easy. In this case, however, the debug features of the Snapdragon 820 were intentionally disabled per implementation agreement between the board supplier and the DUT manufacturer [6].

III. Test Setup

A. Device Information

Testing was performed on the Qualcomm Snapdragon 820 using Intrinsyc Open-Q™ 820 Development Kits. The device under test (DUT) is the Snapdragon 820 SOC which is positioned under a heat sink (which was removed before irradiation). As stated above, there is a low power double data rate 4 (LP DDR4) dynamic random access memory (DRAM) mounted on top of the DUT in the POP configuration. This device does not have bond balls between the DUT die and the DDR4 die (it is only soldered on with pins on the periphery).

The heat sink was removed before testing, but the DDR4 could not be removed without disabling the system. Thus, we needed the heavy ion beam to traverse the DDR4 and the Snapdragon dies. The Snapdragon is assumed to be in flip-chip configuration, but this was not verified. The test results do show the ions clearly affect the sensitive region of the processor. It should be noted that it is a relatively easy job to determine all the die thicknesses and positions, but we were not able to line up resources and sacrificial test boards during this effort and were forced to estimate values based on our test results and best guesses.

B. Beam Information

Heavy ion testing was performed at TAMU in September 2016 and July 2017. Proton testing was performed at MGH in October 2016, and neutron testing was performed at LANSCE in December 2016.

For neutron and proton testing, the particle energies were sufficient to be essentially unaffected by the stack of materials before the sensitive region of the DUT. For heavy ion testing, the stack up of materials was estimated as given in Table I, below. Note that this table has a column for the low and high density and thickness estimates based on the test engineer's experience with similar devices to the DDR4 LP and Snapdragon 820.

Table I: The materials stack used as an estimation for the Snapdragon 820 and LP DDR4 stack of materials. The aramica and air thicknesses were known exactly.

		Range of Thicknesses	
Item	Matrial	Low	High
Beam Port	Aramica	25.4 µm	
Air	Air	3 cm	
DDR3 Top Plastic	Plastic	100 µm (1.18 g/cm^3)	300 µm (1.85 g/cm^3)
DDR3 Die	Silicon	250 µm	400 µm
DDR3 Metalization	Aluminum	40 µm	60 µm
Air Gap	Air	100 µm (1.18 g/cm^3)	300 µm (1.85 g/cm^3)
Snapdragon Top Plastic	Plastic	100 µm	300 µm
Snapdragon Die	Silicon	500 µm	800 µm

C. Test System

For early heavy ion testing, the test boards were powered with a laboratory power supply that provided the 5 V supply to the board. Since no issues were observed with the early heavy ion testing, we only used the manufacturer supplied power supplies for proton and neutron testing, as well as later heavy ion testing (it should be noted that we had no method to monitor the actual power rails of the DUT due to the board construction). The lab power supply was remotely controlled and monitored. Any significant increase in current could be used to stop the irradiation. But no significant increases were ever observed. For sake of clarity, this power supply setup is anecdotal at best, but it is the only viable solution we had.

The DUT was connected by two USB ports to a test computer. The first USB port provided the Android debug bridge (ADB) connection that could be used to upload alternate test software. The second USB port provided a serial connection to the DUT providing a terminal connection to Android (note that Android outputs to a serial console, as enabled in the test boards).

A simple switch was run over a Bayonet Neill-Concelman (BNC) connector and connected to the board power button. This switch, when closed, was equivalent of pressing the power button on the DUT board.

For neutron testing, the system was modified somewhat to allow automation of the entire test approach during over-night operations with no on-site monitoring. We were able to detect incorrect operation (crashes, fail to boot due to stuck bits, and other deviations from expected data rates) through monitoring of output log file data rates. Once the data rate failed to be within tolerance for a given stage of operation, the test system would cycle power, press the power switch, break into the boot sequence, and upload the desired test software.

D. Test Software

Two primary test software types were used. One performs the entire test before any of the Android operating system starts. This renders it unable to perform I/O till a later time when Android enables I/O ports, and can crash for a multitude of reasons between the radiation exposure and the actual start of Android. A second test type, developed after the initial heavy ion tests, performs the SEE test after Android has brought up the I/O system, and provides immediate information about SEEs, however it also invokes Android's handling of many of the exception states in the device and obscures the results.

Crashes are a significant fraction of all observed behaviors during exposure. The tests that used the first software type were unable to provide any useful information about the device and were very frustrating to run. So this approach was scrapped very early in the proton testing.

The second test algorithm was used to develop a few specific test capabilities. During-test development was used to improve test capabilities (using in-situ beam to improve test capability – which was supported under research efforts supported by LANSCE and would not have been possible under normal programmatic test efforts). The proton, neutron, and second heavy ion tests also feature write/read tests of various sizes from 16 kB to 256 kB. An additional read test that can observe 1 GB of the LP DDR4 to determine if bits flipped during irradiation was also used. Sizes over 256 kB ran into memory management unit (MMU) problems with the Android architecture which is very protective of memory boundaries and did not allow our test algorithms to write to memory even though they were running as kernel code.

E. Stuck Bits

Stuck bits were observed in two places during testing. One was in the test program, where we intentionally monitored for incorrect bits. The other is discussed in the next paragraph. It is important to note that Android, by default, fills all memory that gets allocated. And the kernel boot allocates all memory (though it may release the memory immediately). This means that there was a fixed pattern that was observable throughout 1 GB of continuous memory. Our test software did not control the memory allocation, and by default Android allocates memory in a random fashion. Thus, it was serendipitous or lucky that 1 GB of contiguous memory could be read. It was not, however, writable, and thus we could not do anything about putting any other desired pattern in.

A second means of detecting stuck bits comes in the memory allocation system itself, and involves Android detecting a bit error. During boot, a system with stuck bits poses potential problems for Android. First, an error could potentially show up in a critical boot item. Second, an error could show up during allocation of a memory resource. And, finally, a bit error could be found during background testing and setup. In the first case, a stuck bit in a critical item for boot is likely to cause boot to fail, possibly with no indication of what is wrong. Alternately, a bit error can be found during memory allocation because the allocation system in our Android installations actively tests memory when it is allocated. If a stuck bit occurs during allocation, the allocation system returns a failure code. It is then up to the individual algorithm requesting the memory to determine how to proceed. In the final case, we also observed that all remaining memory is initialized with a known pattern. In this remaining memory, bit errors are not reported during boot. However, the memory can be checked by a test algorithm and deviation from the expected value can be reported.

IV. Heavy Ion Test Results

This section provides heavy ion test results for both the Snapdragon 820 and the Hynix DDR4 device.

A. Single-Event Latchup

We monitored for SEL, but did not have a significantly well-instrumented power delivery system to the DUT. Instead, we monitored board-level current delivery. Although there were significant changes in the board-level current delivered, there was no evidence of an increase in overall board current that did not recover by itself. The exposure levels with no distinguishable SEL event were as given in Table II below.

Table II: Total beam delivered for establishing SEL test effectiveness.:

Beam	LET (MeV-cm^2/mg)	Exposure (cm^2)
N	1	1.2E+07
Ne	6	4.4E+06
Ar	15	1.7E+06

It should be noted that it is possible there is built-in current limiting in the test board that would cause an SEL condition to not be allowed. This means that the SEL test is inconclusive for the DUT, but indicates at least a built-in protection system for the test board.

B. Crashes

We use a general definition of crash as "the system does not continue executing code as expected. This includes that we cannot recover interaction by repeatedly pressing keys (on the DUT serial interface). In addition, we refer to it as a crash if the DUT reboots by itself.

We developed crash data at all tested LETs, though with the Ne beam (LET ~6 MeV-cm^2/mg), the data are somewhat limited. The results are shown in Fig. 3, below.

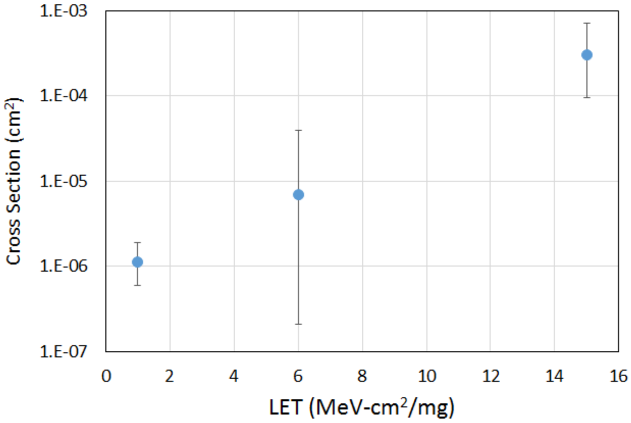

Figure 3: Cross section for crashes of Snapdragon 820 DUTs during heavy ion exposure.

C. *Registers*

Using the test code that was injected into a working Android boot loader, we tested for register bit errors. 20 registers were tested, each containing 64 bits of data. Only one bit error was seen in one of the tested registers (total of 1280 bits) throughout all testing. That bit error occurred at LET 15 MeV-cm^2/mg. As a result, we have the limiting cross sections and single data point in Fig. 4, below.

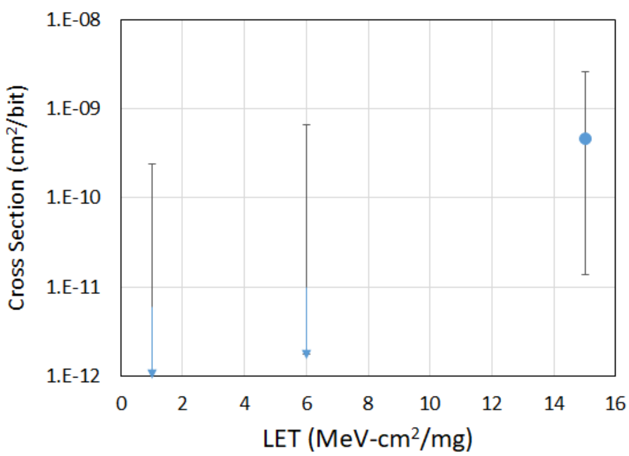

Figure 4: Limiting cross section for register SBUs in the Snapdragon 820. The datum at LET 15 MeV-cm^2/mg represents the only point where a bit error was observed in a register.

D. *Memory Bit Errors*

We tested for bit errors in the Snapdragon's on-chip memory using different sizes of tested memory intended to stay in L1 and L2 caches, and to force off-chip memory access. No bit errors were observed in error reports at any level of exposure. As a result, we have the limiting cross section curve in Fig. 5, below.

E. *DDR4 Bit Errors*

With the updated software developed during proton and neutron testing, we were able to obtain bit errors in the DDR4 device when testing with Ne and Ar. It should be noted that DDR devices are tending towards single event functional interrupts (SEFIs) at low LET, rather than bit errors. We think SEFIs in the DDR4 device are causing many of the crashes, but they are not observable. The cross section for DDR4 SBUs is given in Fig. 6 below.

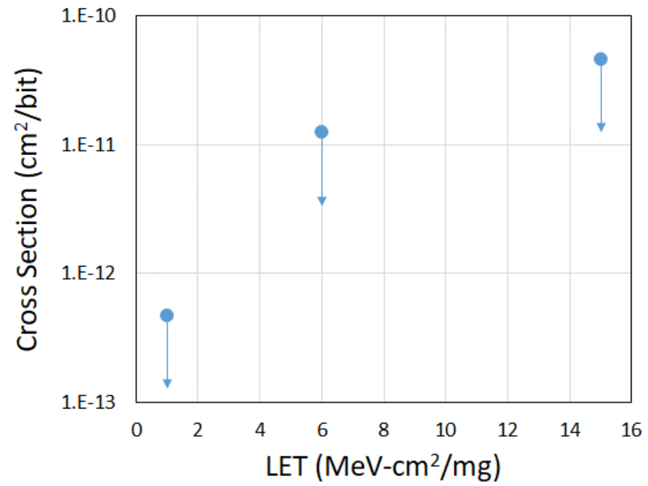

Figure 5: Limiting cross section for memory SBUs in the Snapdragon 820.

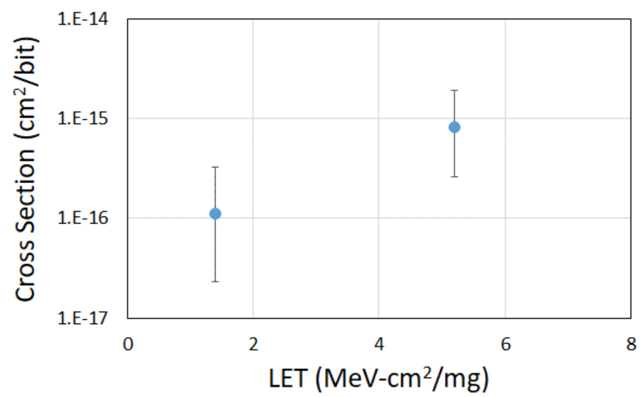

Figure 6: Cross section for SBUs in the Hynix DDR4 device. Note these are read-only and may reflect a percentage of bits that are not upsettable due to the value stored in them.

F. *Stuck Bits*

Test boards used in heavy ion testing were the same ones used in neutron and proton testing and had intrinsic stuck bits we could not remove. These provided a background of a few bits that would toggle in and out of being observed but are not believed to be caused by heavy ion exposure. No true stuck bits were believed to be caused by heavy ion tests. The limiting cross section due to exposure with heavy ions on the DDR4 devices was 2.6×10^{-17} cm^2/bit at LET 0.9 MeV-cm^2/mg, 7.1×10^{-17} cm^2/bit at LET 1.4 MeV-cm^2/mg, and 1.9×10^{-16} cm^2/bit at LET 5.2 MeV-cm^2/mg.

G. *Strange Events*

We observed an interesting set of exception messages before the Snapdragon 820 either crashed or did other things (in some cases becoming more stable – we think due to the death of Android software threads that were increasing crash sensitivity). We determined that some of the events came from CPU cores other than the tested core. This information can potentially be used to improve SEE sensitivity of test algorithms and possibly any flight software.

Some messages we observed:

- Attempted reset with no indication why (might be due to watchdog)
- TS1 Mode in Synchronous Abort handler detected
- Unhandled fault: synchronous external abort
- L2 correctable parity error (after this exception, device operated nominally for relatively long time)
- Unhandled fault: synchronous abort (translation table walk)

V. Proton Results

A. Crashes

The Snapdragon 820 manifested crashes with protons. A total of 23 crashes were observed across three proton energies. Results are shown in Fig. 7, below.

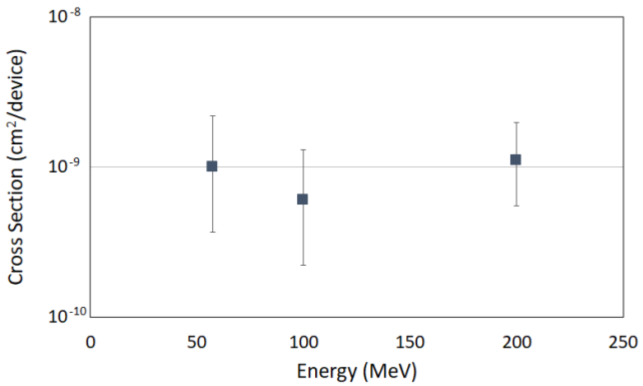

Figure 7: Proton sensitivity of the Open-Q Snapdragon 820 boards to crashes

B. Registers

No changes in any test registers were observed during proton testing. Twenty 64-bit registers were tested, and a limiting cross section of 2.4×10^{-14} cm^2/bit was established due to no events in a total exposure of 1.2×10^{-11}/cm^2 across all energies.

C. Memory Bit Errors

SBUs in the off-chip DDR4 LP were observed. Generally speaking, the number of SBUs is very similar to the number of stuck bits. In the case of proton testing it is possible that stuck bits are about ten times more likely than actual bit errors. Please see the next section for a discussion of stuck bits. Because these cannot be separated, we do not claim a particular proton memory bit error cross section.

D. Stuck Bits

We observed stuck bits during proton testing. The cross section for stuck bits as a function of energy is provded in Fig. 7. Note that for Board 3, the low energy point was taken late in the data collection and may include a large amount of higher-energy stuck bits contaminating the result (pushing the data point higher).

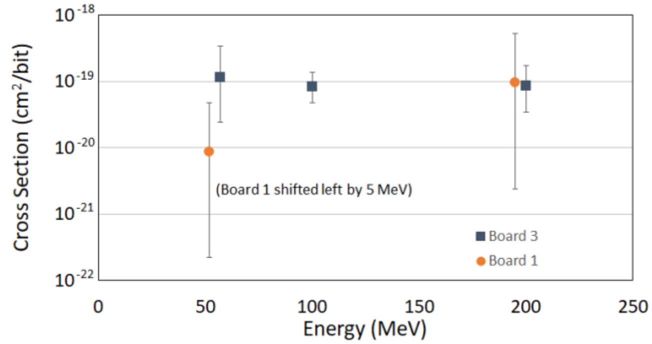

Figure 8: Stuck bit sensitivity of the DDR4 device. Results are shown for two boards.

VI. Neutron Results

Additional data was taken with neutrons at LANSCE. Testing at LANSCE provided a unique opportunity to improve the data collection methods and algorithms, due to the nature of the test environment and the support of the test facility (please see the acknowledgement). General results for the neutron testing are the following:

1) *The same general response as for the proton testing – crashes and stuck bits were the dominant error types*

2) *We were able to modify the custom software to restart after Android's exception handling caught an exception, but it is not clear that this creates a repeatable test environment relative to the running state before an exception is observed*

3) *The cross section for crashes and stuck bits was about the same, at 1×10^{-9}cm^2/device. This corresponds to approximately 1×10^{-19}cm^2/bit for stuck bits. These are also consistent with the proton results.*

4) *Stuck bits were successfully annealed during the course of the experiment to enable continued exposure when stuck bits could result in failure to boot.*

VII. Conclusion

The Qualcomm Snapdragon 820 and its support DDR4 LP device from SK Hynix (H9HKNNNDGUMUBR-NMH) were tested for SEE with heavy ions, protons, and neutrons, in order to establish the general SEE performance of the Snapdragon DUT. Test development proved very difficult and resulted in data with limited ability to be applied to general structures. However, the data were taken using the Android kernel as a test platform and results are expected to be consistent with general use cases.

We did not observe any permanent damage to the DUTs, however we did have significant problems with stuck bits, and the permanent-damage-test estimated maximum LET is 15 MeV-cm^2/mg, with a limiting cross section of about 1×10^{-3} cm^2 (limited by our desire to observe functionality during testing; there is no reason to think the DUTs might have significant damaging errors just above the threshold level at which we tested.

Register- and memory- bit errors were tested for, with the heavy ion test program observing only a single register bit error (partially due to the limited number of bits tested [~30 kB] compared with the proton and neutron tests which sensitized ~1 GB of off-chip LP DDR4, which did show bit errors). Proton testing, on the other hand, observed proton SEEs in the off-chip memory (the DDR4 LP device), however, these upsets were mixed with stuck bits and it is not generally possible to separate these two phenomena.

VIII. Acknowledgment

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